ABSTRACT

Imprint Suppression Circuit Scheme

A ferroelectric memory array includes a plurality of memory pages each formed of a plurality of ferroelectric memory cells. The ferroelectric memory cells are supplied by common word lines. Status memory cells are connected to each of the plurality of memory pages, each status memory cell stores the status of the memory page to which it is connected. A plurality of sense amplifiers each receives inputs from a pair of bit lines. Each of the bit lines receives inputs from the ferroelectric memory cells of a plurality of the memory pages. The sense amplifiers write back data into the memory cells and status cells in reversed states following read operations.